IN THE CLAIMS

1. (currently amended) A vertical NROM memory cell comprising:

a plurality of oxide pillars each having a source/drain region, a trench being formed between each pair of oxide pillars ~~pillar~~;

a control gate formed between each pair of oxide pillars;

a plurality of program gates, each formed between the control gate and each oxide pillar, each program gate extending along the oxide pillar sidewall; and

a plurality of gate insulator layers, each gate insulator layer formed between each program gate and the adjacent oxide pillar, each gate insulator layer having a structure for trapping at least one charge.

2. (Original) The memory cell of claim 1 wherein the source/drain region is formed at the top of each pillar.

3. (Original) The memory cell of claim 1 wherein the plurality of gate insulators are comprised of a composite oxide-nitride-oxide structure such that the nitride layer the charge trapping structure.

4. (Original) The memory cell of claim 1 and further including a silicon oxide gate insulator formed between the control gate and the adjacent program gates and along the bottom of the trench.

5. (Original) The memory cell of claim 1 wherein each gate insulator layer is a composite layer comprised of one of an oxide-nitride-aluminum oxide composite layer, an oxide-aluminum oxide-oxide composite layer, or an oxide-silicon oxycarbide-oxide composite layer.

6. (Original) The memory cell of claim 1 wherein each gate insulator layer is a non-composite layer comprised of one of silicon oxides formed by wet oxidation and not annealed, silicon-rich oxides with inclusions of nanoparticles of silicon, silicon oxynitride layers, silicon-rich aluminum oxide insulators, silicon oxycarbide insulators, or silicon oxide insulators with inclusions of nanoparticles of silicon carbide.

7. (Original) The memory cell of claim 1 wherein each gate insulator is comprised of non-stoichiometric single layers of two or more of silicon, nitrogen, aluminum, titanium, tantalum, hafnium, lanthanum, or zirconium.

8. (Original) A vertical NROM memory cell comprising:
a plurality of oxide pillars each having a source/drain region formed at the top, a trench being formed between each pair of oxide pillars;
a control gate formed between each pair of oxide pillars;
a plurality of program gates, each formed between the control gate and each oxide pillar, each program gate extending along the oxide pillar sidewall;
a plurality of gate insulator layers, each gate insulator layer formed between each program gate and the adjacent oxide pillar sidewall, each gate insulator layer having a structure for trapping at least one charge; and
an oxide interpoly layer formed between the control gate and each adjacent program gate.

9. (Original) The memory cell of claim 8 and further including a gate insulator layer formed on the bottom of the trench such that a plurality of charges can be trapped under the control gate in the gate insulator layer.

10. (Original) The memory cell of claim 9 wherein the plurality of charges are trapped in a nitride layer of the gate insulator layer under the control gate.

11. (Original) An array of vertical NROM memory cells comprising:
a plurality of oxide pillars each having a source/drain region formed at the top, a trench being formed between each pair of oxide pillars;
a plurality of control gates, each control gate formed in the trench between each pair of oxide pillars;
a plurality of program gates, each formed in the trench between a first control gate and each oxide pillar, each program gate extending along the oxide pillar sidewall;
a plurality of gate insulator layers, each gate insulator layer formed between each program gate and the adjacent oxide pillar, each gate insulator layer having a structure for trapping at least one charge; and
a word line coupling the plurality of control gates.

12. (Original) The array of claim 11 and further including:

    an oxide interpoly material between each control gate and each program gate; and

    a gate insulator layer on the bottom of each trench and comprising a structure for storing a plurality of charges under each control gate.

13. (Original) The array of claim 11 wherein each source/drain region is comprised of an n-type conductivity semiconductor material.

14. (Original) A computer system, comprising:

    a central processing unit (CPU); and

    an array of vertical NROM memory cells coupled to the CPU, the array including:

        a plurality of oxide pillars each having a source/drain region formed at the top, a trench being formed between each pair of oxide pillars;

        a plurality of control gates, each control gate formed in the trench between each pair of oxide pillars;

        a plurality of program gates, each formed in the trench between a first control gate and each oxide pillar, each program gate extending along the oxide pillar sidewall;

        a plurality of gate insulator layers, each gate insulator layer formed between each program gate and the adjacent oxide pillar, each gate insulator layer having a structure for trapping at least one charge; and

        a word line coupling the plurality of control gates.

15. (Original) The computer system of claim 14 wherein the source/drain region of each oxide pillar acts as either a source connection or a drain connection in response to a direction of operation of the vertical NROM memory cell.

16. (Original) The computer system of claim 14 wherein each second source/drain region is comprised of an N+ conductivity silicon material.

17. (Original) A method for forming a vertical NROM split gate transistor, the method comprising:

forming a first columnar structure on a substrate, the first columnar structure having a doped region of a first type of conductivity that is different than the substrate;

forming a second columnar structure on the substrate that is spaced apart from the first columnar structure to form a trench between the two columnar structures, the second columnar structure having a doped region of the first type of conductivity;

forming an oxide material on the bottom of the trench;

forming a polysilicon control gate structure between the first and second columnar structures;

forming a first gate insulator layer in the trench along the sidewall of the first columnar structure and a second gate insulator layer in the trench along the sidewall of the second columnar structure; and

interposing a polysilicon program gate structure between the first gate insulator layer and the control gate structure and between the second gate insulator layer and the control gate structure.

18. (Original) The method of claim 17 and further including forming an oxide interpoly region between the control gate structure and the program gate structures.

19. (Original) The method of claim 17 wherein the first type of conductivity is N+ and the substrate has a P+ conductivity.

20. (Original) The method of claim 17 wherein forming the first and second gate insulator layers comprises forming a composite oxide-nitride-oxide layer.

21. (Original) A method for forming a vertical NROM split gate transistor, the method comprising:

forming a first columnar structure on a substrate, the first columnar structure having a doped region of a first type of conductivity that is different than the substrate;

forming a second columnar structure on the substrate that is spaced apart from the first columnar structure to form a trench between the two columnar structures, the second columnar structure having a doped region of the first type of conductivity;

forming a bottom gate insulator layer on the bottom of the trench;

forming a polysilicon control gate structure between the first and second columnar structures;

forming a first gate insulator layer in the trench along the sidewall of the first columnar structure and a second gate insulator layer in the trench along the sidewall of the second columnar structure; and

interposing a polysilicon program gate structure between the first gate insulator layer and the control gate structure and between the second gate insulator layer and the control gate structure.

22. (Original) The method of claim 21 wherein the bottom, first, and second gate insulator layers are a composite structure.

23. (Original) The method of claim 22 wherein the composite structure is comprised of one of an oxide-nitride-aluminum oxide composite layer, an oxide-aluminum oxide-oxide composite layer, or an oxide-silicon oxycarbide-oxide composite layer.

24. (Original) The method of claim 21 wherein the bottom, first, and second gate insulator layers are comprised of non-stoichiometric single layers of two or more of silicon, nitrogen, aluminum, titanium, tantalum, hafnium, lanthanum, or zirconium.

25. (Original) The method of claim 21 wherein the bottom, first, and second gate insulator layers are non-composite layers comprised of one of silicon oxides formed by wet oxidation and not annealed, silicon-rich oxides with inclusions of nanoparticles of silicon, silicon oxynitride layers, silicon-rich aluminum oxide insulators, silicon oxycarbide insulators, or silicon oxide insulators with inclusions of nanoparticles of silicon carbide.